

HCIA-5G-RNP&RNO V2.0

Huawei H35-580 V2.0

Version Demo

Total Demo Questions: 2

Total Premium Questions: 23

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Topic Break Down

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Topic 2, 5G RAN Basics	7
Topic 3, 5G RAN Planning	3
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QUESTION NO: 1

Which KPI observations provide evidence of an uplink coverage weakness in an NR cell? (Select two)

- A. Low PUSCH SINR at the cell edge.
- B. High timing advance together with an elevated PUSCH BLER.
- C. High DL PRB utilization during the busy hour.
- D. Low PDSCH BLER for users served by the cell.
- E. High downlink rank indication reported by UEs.

ANSWER: A B

Explanation:

Low PUSCH SINR at the cell edge and **high timing advance together with an elevated PUSCH BLER** provide evidence of uplink coverage weakness. Low uplink SINR and high uplink block-error rate show that the gNodeB is receiving a weak or impaired uplink signal. High timing advance indicates a larger UE-to-site propagation distance and strengthens the cell-edge interpretation. High DL PRB utilization indicates downlink resource loading, and low PDSCH BLER reflects good downlink transmission reliability rather than an uplink coverage problem.

QUESTION NO: 2

Adjacent TDD NR cells use different downlink-to-uplink slot directions at the same time. UEs near the cell border experience uplink degradation even though uplink coverage is otherwise adequate. Which action is most appropriate?

- A. Align the TDD frame configuration and time synchronization.
- B. Increase the UE maximum uplink transmit power.
- C. Replan the NR PCI of the affected cells.
- D. Expand the tracking area of the border cells.

ANSWER: A

Explanation:

Align the TDD frame configuration and time synchronization is correct. Different slot directions in adjacent TDD cells can create cross-link interference, such as a downlink transmission from one cell interfering with uplink reception in another cell. Coordinating the TDD pattern and maintaining accurate time synchronization reduces this interference. Increasing UE transmit power does not remove downlink-to-uplink cross-link interference, and changing PCI or tracking-area configuration is unrelated to TDD slot-direction conflicts.